(b.) applying and curing spin-on glass, to form a first dielectric layer;

(c.) depositing dielectric material under vacuum conditions, to form a second dielectric layer over said first layer, said second dielectric layer having a thickness equal to or less than said first layer;

(d.) applying and curing spin-on glass, to form a dielectric stack including a third dielectric layer over said first and second layers, said third dielectric layer having a thickness equal to or greater than said second layer;

(e.) performing a global etchback to substantially remove said dielectric stack from said high points of said partially fabricated structure;

(f.) deposition of an interlevel dielectric;

(g.) etching holes in said interlevel dielectric in locations; and

(h.) depositing and patterning a metallization layer to form a pattern of connections, including connections through said holes.

16. The method of claim **15**, wherein said deposition step (c.) is plasma-enhanced.

17. The method of claim **15**, wherein said deposition step (c.) uses TEOS as a source gas.

18. The method of claim **15**, comprising the additional step of applying a passivating dielectric, under vacuum conditions, after said step (a.) and before said deposition step (b.).

19. The method of claim **15**, wherein said deposition step (b.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

20. The method of claim **15**, wherein said interlevel dielectric is a doped silicate glass.

21. The method of claim **15**, wherein said deposition step (d.) applies said spin-on glass with a thickness in the range of 1000–5000 Å inclusive.

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